

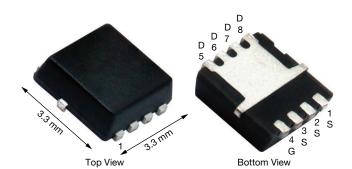
BSZ240N12NS3 G-VB Datasheet N-Channel 100 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	100				
$R_{DS(on)}$ Typ. (Ω) at $V_{GS} = 10 \text{ V}$	0.0174				
$R_{DS(on)}$ Typ. (Ω) at $V_{GS} = 7.5 \text{ V}$	0.0205				
Q _g typ. (nC)	15.1				
I _D (A)	35.3 ^{a, g}				
Configuration	Single				

FEATURES

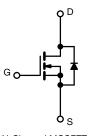
- Trench Gen IV power MOSFET
- Very low R_{DS} Q_g figure-of-merit (FOM)
- \bullet Tuned for the lowest R_{DS} Q_{oss} FOM
- 100 % R_g and UIS tested





APPLICATIONS

- · Synchronous rectification
- Primary side switch
- DC/DC converter
- · Motor drive switch
- · Battery and load switch
- Industrial



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100	V	
Gate-source voltage		V _{GS}	± 20	v	
	T _C = 25 °C		35.3		
Continuous drain surrent (T = 150 °C)	T _C = 70 °C	1 .	28.2		
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	- I _D	9.4 b, c		
	T _A = 70 °C	† †	7.5 ^{b, c}	^	
Pulsed drain current (t = 100 μs)		I _{DM}	80	A	
Continuous source-drain diode current	T _C = 25 °C		47.2		
	T _A = 25 °C	3.3 b, c			
Single pulse avalanche current	L = 0.1 mH	I _{AS}	20		
Single pulse avalanche energy	L = 0.1 IIII	E _{AS}	20	mJ	
Maximum power dissipation	T _C = 25 °C		52		
	T _C = 70 °C	T 5	33.3	w	
	T _A = 25 °C	P _D	3.7 b, c	VV	
	T _A = 70 °C		2.4 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^c			260		

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	24	33	°C/W		
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.9	2.4	- C/W		

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- d. The DFN3x3 package is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 81 °C/W
- g. $T_C = 25$ °C



PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	$I_{\rm J}$ $I_{\rm D}$ = 10 mA		81	-	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-7.5	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	-	4	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA
		V _{DS} = 100 V, V _{GS} = 0 V	-	-	1	μΑ
Zero gate voltage drain current	IDSS	V _{DS} = 100 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α
Delice and a state and the second	Б	V _{GS} = 10 V, I _D = 10 A	-	0.0174	_	Ω
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	-	0.0205	_	
Forward transconductance a	9 _{fs}	V _{DS} = 15 V, I _D = 10 A	-	46	-	S
Dynamic ^b						
Input capacitance	C _{iss}		-	1470	-	
Output capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	132	-	pF
Reverse transfer capacitance	C _{rss}		-	11.2	-	
Total gate charge	Q _g	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	20	30	
		30 7 40 7 5	-	15.1	22.7	nC
Gate-source charge	Q _{as}	$V_{DS} = 50 \text{ V}, V_{GS} = 7.5 \text{ V}, I_{D} = 10 \text{ A}$	-	6.45	-	
Gate-drain charge	Q_{gd}		-	3.5	-	
Output charge	Q _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	22	-	
Gate resistance	Rq	f = 1 MHz	0.2	0.76	1.4	Ω
Turn-on delay time	t _{d(on)}		-	12	24	
Rise time	t _r	$V_{DD} = 50 \text{ V}, R_{I} = 5 \Omega, I_{D} \approx 10 \text{ A},$	-	5	10	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	19	38	
Fall time	t _f		-	5	10	1
Turn-on delay time	t _{d(on)}		-	15	30	ns
Rise time	t _r	$V_{DD} = 50 \text{ V}, R_L = 5 \Omega, I_D \cong 10 \text{ A},$	-	6	12	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	19	38	
Fall time	t _f		-	5	10	1
Drain-Source Body Diode Characteristi	cs					
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	47.2	
Pulse diode forward current	I _{SM}	-	-	-	80	- A
Body diode voltage	V _{SD}	$I_S = 5 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.78	1.1	V
Body diode reverse recovery time	t _{rr}		-	43	86	ns
Body diode reverse recovery charge	Q _{rr}		-	72	144	nC
Reverse recovery fall time	ta	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 \text{ °C}$	-	33	-	1
Reverse recovery rise time	t _b		_	10	_	ns

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

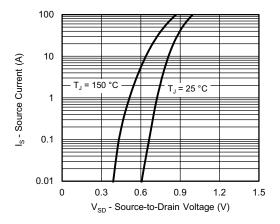
Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

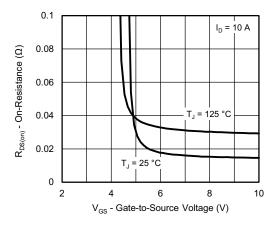
Capacitance



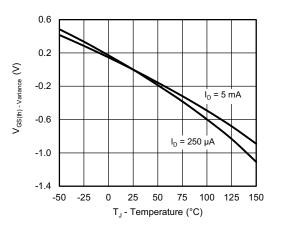
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



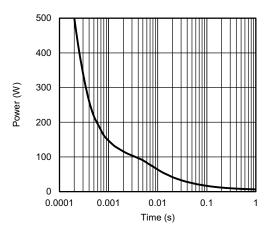
Source-Drain Diode Forward Voltage



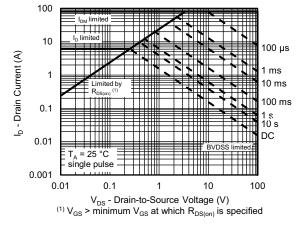
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

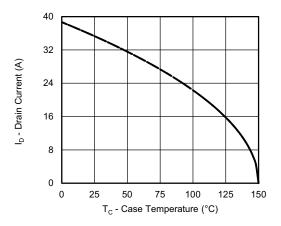


Safe Operating Area, Junction-to-Ambient

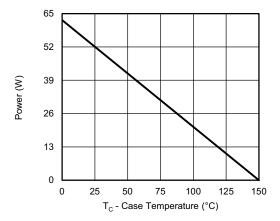
4 服务热线:400-655-8788

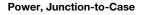


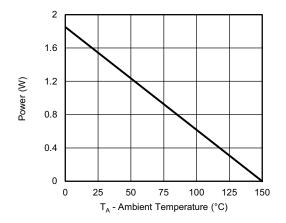
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating a







Power, Junction-to-Ambient

Note

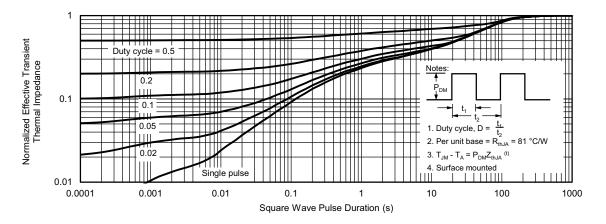
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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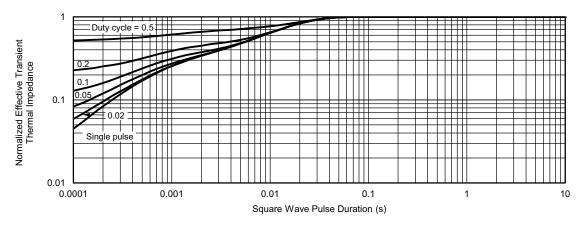
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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